1. A micro mirror array comprising:

an upper wafer portion including a plurality of movable reflective surfaces located thereon, said upper wafer portion defining a coverage area in top view; and

a lower wafer portion located generally below and coupled to said upper wafer portion, said lower wafer portion including at least one connection site located thereon, said at least one connection site being electrically or operatively coupled to at least one component which can control the movement of at least one of said reflective surfaces, said at least one connection site generally not being located within said coverage area of said upper wafer portion.

2. The array of claim 1 wherein said lower wafer portion includes a plurality of connection sites, each of said connection sites being electrically or operatively coupled to a component which can control the movement of at least one of said reflective surfaces, wherein each connection site is not generally located within said coverage area of said upper wafer portion.

3. The array of claim 2 each of said components is an electrode located on said lower wafer portion for controlling the movement of at least one movable reflective surface when a voltage or current is applied across said at least one movable reflective surface and said electrode.

4. The array of claim 3 wherein at least two electrodes are located below each of said reflective surfaces such that a voltage can be applied across each of said electrodes and an associated reflective surface to cause the associated reflective surface to move in at least two generally opposite directions.

5. The array of claim 3 wherein each reflective surface is located on a movable portion such that when a voltage is applied across an associated electrode and said reflective surface or said movable portion such voltage causes movement of the associated movable portion and of the associated reflective surface.

6. The array of claim 2 wherein said connection sites can carry sufficient bandwidth to enable a controller coupled to said connection sites to cause and control the individual movement of each reflective surface relative to any adjacent reflective surfaces.

7. The array of claim 1 wherein said at least one connection site includes a solderable surface configured to receive an electronic component thereon in a direct attachment manner.

8. The array of claim 7 wherein said at least one connection site is electrically or operatively coupled to a component which can control the movement of at least one of said reflective surfaces.

9. The array of claim 7 wherein said at least one connection site has a melting point of less than about 250°C.

10. The array of claim 7 further including a chip or electronic component electrically or operatively coupled to and supported by said at least one connection site such that said chip or electronic component can control the movement of at least one of said movable reflective surfaces.

11. The array of claim 10 wherein said chip or electronic component is a flip chip that is coupled to said connection site by flip chip bonding.

12. The array of claim 10 further comprising a controller coupled to said chip or electronic component to provide control signals passed to said connection site by said chip or electronic component to thereby control the movement of said at least one reflective surface.

13. The array of claim 7 wherein said at least one connection site includes a plurality of conductive pads, each pad being electrically isolated from any adjacent pads.

14. The array of claim 1 wherein said lower wafer portion has a coverage area in top view and wherein said coverage area of said upper wafer portion is entirely contained within said coverage area of said lower wafer portion.

15. The array of claim 1 wherein said upper wafer portion includes an outer perimeter in top view, and wherein said at least one connection site is located adjacent to said outer perimeter.

16. The array of claim 1 wherein said upper wafer portion includes an outer perimeter, and wherein said outer perimeter defines said coverage area.

17. The array of claim 1 wherein said upper and lower wafer portions are coupled together by a photopatternable adhesive.

18. The array of claim 17 wherein said photopatternable adhesive is benzocyclobutene.

19. The array of claim 1 wherein said upper and lower wafer portions are coupled together by a relatively low temperature adhesive, said adhesive having a reflow temperature of less than about 125° C.

20. The array of claim 1 wherein each reflective surface is individually movable relative to any adjacent reflective surface and is individually controllable.

21. The array of claim 1 wherein said upper wafer portion includes a silicon layer, and wherein said reflective surfaces are located on, adjacent to, or supported by said silicon layer.

22. The array of claim 1 wherein said upper wafer portion includes a base portion and a plurality of movable portions rotatably coupled to base portion, and wherein each reflective surface is located on one of said movable portions.

23. The array of claim 1 wherein said upper wafer portion includes at least a portion of at least one silicon-on-insulator wafer.

24. The array of claim 1 wherein each reflective surface is independently movable about two generally perpendicular axes.

25. The array of claim 1 wherein said lower wafer portion is or includes at least part of a semiconductor wafer, or a ceramic substrate, or a glass substrate, or a printed circuit board.

26. The array of claim 1 wherein said lower wafer portion includes an upper surface facing said upper wafer portion, and wherein said at least one connection site is located on said upper surface.

27. A micro mirror array comprising:

an upper wafer portion including a plurality of movable reflective surfaces located thereon; and

a lower wafer portion located generally below and coupled to said upper wafer portion, said lower wafer portion including a plurality of components which can control the movement of said reflective surfaces, said lower wafer portion including at least one electronic component located thereon which is electrically or operatively coupled to at least one of said components such that said electronic component can control the movement of at least one of said movable reflective surfaces located adjacent to said at least one of said components.

28. A microstructure system including:

a wafer portion including a microstructure formed therein, located thereon or supported thereby; and

a solderable surface configured to receive an electronic component thereon in a direct attachment manner, said solderable surface being formed on, located on, or supported by

said wafer portion, said solderable surface being electrically or operatively coupled to said microstructure such that an electronic component coupled to solderable surface can control, operate or receive inputs from at least part of said microstructure.

29. The microstructure system of claim 28 wherein said wafer portion includes an upper wafer portion and a lower wafer portion located generally below and at least partially spaced apart from said upper wafer portion, and wherein said microstructure is formed in or located on said upper wafer portion, and wherein said solderable surface is formed or located on said lower wafer portion.

30. The microstructure system of claim 29 wherein said upper wafer portion defines a coverage area in top view, and wherein said solderable surface is not located within said coverage area.

31. The microstructure system of claim 30 wherein said upper wafer portion includes an outer perimeter, and wherein said outer perimeter defines said coverage area.

32. The microstructure system of claim 30 wherein said lower wafer portion has a coverage area in top view and wherein said coverage area of said upper wafer portion is entirely contained within said coverage area of said lower wafer portion.

33. The microstructure system of claim 28 wherein said wafer portion includes an upper wafer portion and a lower wafer portion located generally below and at least partially spaced apart from said upper wafer portion, and wherein said microstructure is formed in or located on one of said upper or lower wafer portions, and wherein said solderable surface is formed or located on the other of said upper or lower wafer portion, and wherein said upper and lower wafer portions are coupled together.

34. The microstructure system of claim 33 wherein said upper wafer and lower wafer

portions are coupled together by a photopatternable adhesive.

35. The microstructure system of claim 34 wherein said photopatternable adhesive is benzocyclobutene.

36. The microstructure system of claim 33 wherein said upper wafer and lower wafer portions are coupled together by a relatively low temperature adhesive, said adhesive having a reflow temperature of less than about 125° C.

37. The microstructure system of claim 28 wherein said solderable surface is a flip chip connection site configured to receive a chip thereon by flip chip bonding.

38. The microstructure system of claim 28 wherein said solderable surface includes a plurality of conductive pads, each pad being electrically isolated from any adjacent pad and having a melting point of less than about 250°C.

39. The microstructure system of claim 28 further including an electronic component coupled to said solderable surface such that said electronic component can control, provide inputs to or receive outputs from said microstructure

40. The microstructure system of claim 39 wherein said electronic component is a chip and wherein said chip is coupled to said solderable surface by flip chip bonding.

41. The microstructure system of claim 28 further including a plurality of solderable surfaces located on, or supported by said wafer portion, each solderable surface being electrically or operatively coupled to said microstructure.

42. The microstructure system of claim 41 further comprising a plurality of electronic components, each electronic component being coupled to one of said plurality of solderable

surface, the system further including a controller coupled to said electronic components to control the input to or output from said electronic components via said solderable surfaces to thereby control or monitor the input to or output from said microstructure.

43. The microstructure system of claim 28 wherein said microstructure is at least one of a sensor or an actuator.

44. The microstructure system of claim 28 wherein said microstructure is a mirror array including a plurality of movable reflective surfaces.

45. The microstructure system of claim 44 further including at least one component which can control the movement of at least one of said reflective surfaces, wherein said solderable surface is electrically or operatively coupled to said at least one component.

46. The microstructure system of claim 45 wherein said component is an electrode for controlling the movement of said at least one movable reflective surface when a voltage or current is applied across said electrode and said at least one reflective surface.

47. The microstructure system of claim 46 wherein at least two electrodes are located below each of said reflective surfaces such that a voltage can be applied across said electrodes and the associated reflective surfaces to cause the associated reflective surface to move in at least two generally opposite directions.

48. The microstructure system of claim 44 wherein each reflective surface is individually movable relative to any adjacent reflective surfaces and is individually controllable.

49. The microstructure system claim 44 wherein said solderable surface can carry a sufficient bandwidth to allow a controller coupled to said solderable surface to cause and control the individual movement of each reflective surface relative to any adjacent reflective surfaces.

50. The microstructure system of claim 44 wherein said wafer portion includes an upper wafer portion and a lower wafer portion located generally below and at least partially spaced apart from said upper wafer portion, and wherein said mirror array is formed in or located on said upper wafer portion, and wherein said solderable surface is formed in, located on or supported by said lower wafer portion.

51. The microstructure system of claim 50 wherein said upper wafer portion includes a silicon layer, and wherein said reflective surfaces are located on said silicon layer.

52. The microstructure system of claim 50 wherein said upper wafer portion includes a base portion and a plurality of movable portions rotatably coupled to base portion, and wherein each reflective surface is located on one of said movable portions.

53. The microstructure system of claim 50 wherein said upper wafer portion includes at least a portion of at least one silicon-on-insulator wafer.

54. The microstructure system of claim 50 wherein said lower wafer portion is or includes at least part of a semiconductor wafer, or a ceramic substrate, or a glass substrate, or a printed circuit board.

55. The microstructure system of claim 50 wherein said lower wafer portion includes an upper surface facing said upper wafer portion, and wherein said solderable surface is located on said upper surface.

56. A microstructure system including:

an upper wafer or wafer portion including a microstructure formed therein, located thereon or supported thereby, said upper wafer portion defining a coverage area in top view; and

a lower wafer or wafer portion located generally below and coupled to said upper

wafer or wafer portion, said lower wafer or wafer portion including an electronic component located thereon or supported thereby, said electronic component being electrically or operatively coupled to said microstructure such that said electronic component can control, operate or receive inputs from at least part of said microstructure, wherein said electronic component is generally not located within said coverage area of said upper wafer portion.

57. A method for manufacturing a micro mirror array comprising the steps of:

providing an upper wafer or wafer portion including a plurality of movable portions located thereon;

providing a lower wafer or wafer portion;

forming at least one connection site on said lower wafer or wafer portion;

forming a plurality of components on said lower wafer or wafer portion, wherein each component can control the movement of at least one movable portion when located adjacent to one of said movable portions, said connection site being electrically or operatively coupled to at least one of said components;

coupling said upper and lower wafers or wafer portions together to form a wafer stack;

locating a reflective material on each of said movable portions; and

singulating said wafer stack to provide at least one mirror array having at least part of said upper wafer or wafer portion which defines a coverage area in top view, and wherein said connection site of said lower wafer is not located inside said coverage area of said upper wafer.

58. The method of claim 57 wherein said singulating step includes singulating said wafer stack to provide at least two mirror arrays, each mirror array having at least part of said upper wafer or wafer portion which defines a coverage area in top view, and wherein both of said mirror arrays include connection sites not located inside the coverage area of the associated part of said upper wafer or wafer portion.

59. The method of claim 57 wherein said singulating step includes singulating said wafer stack along two dividing lines, each of said dividing lines extending generally perpendicular to said wafer stack, each dividing line including first and second portions that are laterally spaced from each other.

60. The method of claim 59 further including the step of forming a pair of spaced lower singulation cavities in said lower wafer or wafer portion, each of which form one of said first or second portions of one of said dividing lines.

61. The method of claim 60 wherein the method further includes the step of forming a pair of upper singulation cavities in said upper wafer or wafer portion, said upper singulation cavities being generally laterally offset from the associated lower singulation cavities after said coupling step, each of said upper singulation cavities forming the other of said first or second portions of said dividing lines.

62. The method of claim 61 wherein said singulating step includes removing portions of said wafer stack located generally above or below at least one of said upper or lower singulation cavities such that said wafer stack can be singulated along said dividing lines.

63. The method of claim 57 further comprising the step of etching said upper wafer or said upper wafer portion to define a base portion and said plurality of a movable portions movably coupled to said base portion.

64. The method of claim 57 wherein each of said components is an electrode located on said lower wafer or wafer portion for controlling the movement of at least one movable reflective surface when a voltage or current is applied across said electrode and the associated movable reflective surface.

65. The method of claim 57 wherein said at least one connection site is a solderable

surface.

66. The method of claim 57 wherein said at least one connection site includes a flip chip connection site configured to receive a chip thereon in a flip chip attachment manner.

67. The method of claim 57 wherein said at least one connection site has a melting point of less than about 250°C.

68. The method of claim 57 further including the step of electrically coupling a chip to said at least one connection site by flip chip bonding.

69. The method of claim 57 wherein after said singulating step said mirror array has at least part of said lower wafer portion or wafer portion which defines a coverage area in top view, and wherein said singulation step is carried out such that said coverage area of said at least part of said upper wafer or wafer portion is entirely contained within said coverage area of said at least part of said lower wafer or wafer portion.

70. The method of claim 57 wherein said at least part of said upper wafer or wafer portion includes an outer perimeter in top view, and wherein said at least one connection site is located adjacent to said outer perimeter.

71. The method of claim 57 wherein said at least part of said upper wafer or wafer portion includes an outer perimeter, and wherein said outer perimeter defines said coverage area.

72. The method of claim 57 wherein said coupling step including coupling said upper and lower wafers or wafer portions by a photopatternable adhesive.

73. The method of claim 72 wherein said photopatternable adhesive is benzocyclobutene.

74. The method of claim 57 wherein said coupling step includes coupling said upper and lower wafers together using a process entirely taking place at a temperature of less than about 125° C.

75. The method of claim 57 wherein each reflective surface is individually movable relative to any adjacent reflective surface and is individually controllable.

76. The method of claim 57 wherein said at least one connection site can carry sufficient bandwidth to enable a controller coupled to said connection site to cause and control the individual movement of each reflective surface relative to any adjacent reflective surfaces.

77. The method of claim 57 wherein said upper wafer or wafer portion includes a silicon layer, and wherein said movable portions are located on, adjacent to, or supported by said silicon layer.

78. The method of claim 57 wherein each movable portion is independently movable

about two generally perpendicular axes.

79. The method of claim 57 wherein said lower wafer or wafer portion is or includes at least part of a semiconductor wafer, or a ceramic substrate, or a glass substrate, or a printed circuit board.

80. The method of claim 57 wherein said lower wafer or wafer portion includes an upper surface facing said upper wafer or wafer portion after said coupling step, and wherein said at least one connection site is located on said upper surface.

81. A method for manufacturing a microstructure system comprising the steps of:

providing an upper wafer or wafer portion including a microstructure formed therein or located thereon;

providing a lower wafer or wafer portion including a solderable surface configured to receive an electronic component thereon in a direct attachment manner; and

coupling said upper and lower wafer or wafer portions together to form a wafer stack such that said solderable surface is electrically or operatively coupled to at least part of said microstructure such that an electronic component coupled to said solderable surface can control, operate, or receive inputs from at least part of said microstructure.

82. The method of claim 81 further comprising the step of directly attaching an electronic component to said solderable surface.

83. The method of claim 81 wherein said solderable surface is a flip chip connection site that is configured to receive a chip thereon in a flip chip attachment manner.

84. The method of claim 83 further including the step of coupling a chip to said flip chip connection site by flip chip bonding.

85. The method of claim 81 wherein said upper wafer or wafer portion defines a coverage area in top view, and wherein said solderable surface is not located within said coverage area after said coupling step.

86. The method of claim 81 wherein said upper wafer or wafer portion includes a plurality of movable portions located thereon, and wherein said lower wafer or wafer portion includes a plurality of components which can control the movement of said movable portions, said solderable surface being electrically or operatively coupled to at least one of said components.

87. The method of claim 86 wherein said components are electrodes located on said lower wafer or wafer portion for controlling the movement of at least one movable portion when a voltage or current is applied across said movable portion and an associated electrode.

88. The method of claim 81 wherein said solderable surface has a melting temperature of less than about 250°C.

89. The method of claim 81 further including the step of coupling a plurality of electronic component to said lower wafer or wafer portion, each electronic component being electrically or operatively coupled to at least part of said microstructure.

90. The method of claim 81 wherein at least one of said upper wafer or wafer portion or said lower wafer or wafer portion includes a silicon layer.

91. The method of claim 81 wherein said lower wafer or wafer portion includes an upper surface facing said upper wafer or wafer portion after said coupling step, and wherein said solderable surface is located on said upper surface.

92. The method of claim 81 further including the step of singulating said wafer stack into

at least two separate wafer stacks.

93. The method of claim 92 wherein said singulating step includes singulating said wafer stack along two dividing lines, each of said dividing lines extending generally perpendicular to said wafer stack, each dividing line including first and second portion that are laterally spaced from each other.

94. The method of claim 92 wherein said upper wafer or wafer portion defines a coverage area in top view, and wherein said singulating step includes singulating said wafer stack such that said solderable surface is not located inside said coverage area of the associated upper wafer or wafer portion.

95. The method of claim 81 wherein said upper wafer or wafer portion includes an outer perimeter in top view, and wherein said solderable surface is located adjacent to said outer perimeter.

96. The method of claim 81 wherein said coupling step including coupling said upper wafer or wafer portion and said lower wafer or wafer portion by a photopatternable adhesive.

97. The method of claim 96 wherein said photopatternable adhesive is benzocyclobutene.

98. The method of claim 81 wherein said coupling step includes coupling said upper and lower wafers together using a process entirely taking place at a temperature of less than about 125° C.

99. A microstructure system comprising:

a microstructure;

at least one lead electrically coupled to said microstructure; and

a first portion of a photopatternable generally electrically insulating material at least partially covering said lead to at least partially electrically isolate said lead, wherein portions of said microstructure are joined together by a second portion of a photopatternable electrically insulating material.

100. The microstructure system of claim 99 wherein said microstructure is a sensor or an actuator.

101. The microstructure system of claim 99 wherein said lead is electrically connected to a component which can cause or sense movement of a movable portion of said microstructure.

102. The microstructure system of claim 99 wherein said first and second portions of said generally electrically insulating layer are the same material.

103. The microstructure system of claim 99 wherein said first and second portions of said generally electrically insulating layer are benzocyclobutene.

104. The microstructure system of claim 99 wherein said first and second portions of said generally electrically insulating layer are different materials.

105. The microstructure system of claim 99 wherein said microstructure is a micro mirror array.

106. The microstructure system of claim 99 wherein said first and second portions of said generally electrically insulating material are located immediately adjacent to each other.

107. A method for manufacturing a microstructure comprising the steps of:

providing a first microstructure portion and a second microstructure portion, at least one of said first or second microstructure portions including at least one lead;

forming a first portion of a photopatternable generally electrically insulating layer at least partially over said lead to at least partially electrically isolate said lead; and

joining said first and second portions of said microstructure together by a second portion of a photopatternable electrically insulating layer.

108. The method of claim 107 wherein said lead is electrically coupled to a movable portion of one of said first or second microstructure portions.

109. A microstructure including:

a first microstructure portion; and

a second microstructure portion, said first and second microstructure portions being joined together by a photopatternable adhesive.

110. The microstructure of claim 109 wherein said photopatternable adhesive is benzocyclobutene.

111. A method for manufacturing a microstructure including the steps of:

providing a first wafer or wafer portion and a second wafer or wafer portion;

locating an adhesive on at least one of said first and second wafers or wafer portions;

patterning said adhesive;

joining said first and second wafer or wafer portions by said adhesive to form a wafer stack; and

machining or etching said wafer stack to form at least one microstructure.

112. The method of claim 111 wherein said adhesive is benzocyclobutene.